GUJARAT TECHNOLOGICAL UNIVERSITY

COMPUTER ENGINEERING (07), INFORMATION TECHNOLOGY (16) & INFORMATION & COMMUNICATION TECHNOLOGY (32)

COMPUTER ORGANIZATION

SUBJECT CODE: 2140707

B.E. 4th SEMESTER

Type of Course: NA

Prerequisite: Basic Understanding of Computer System

Rationale: NA

Teaching and Examination Scheme:

Teaching Scheme			Credits	Examination Marks						Total Marks
L	T	P	C	Theory Marks			Practical Marks			
				ESE (E)	PA (M)		ESE (V)		PA (I)	
					PA	ALA	ESE	OEP		
4	1	0	5	70	20	10	30	0	20	150

Content:

Sr. No.	Topics	Teaching Hrs.	Module Weightage
1	Computer Data Representation Basic computer data types, Complements, Fixed point representation, Register Transfer and Micro-operations: Floating point representation, Register Transfer language, Register Transfer, Bus and Memory Transfers (Tree-State Bus Buffers, Memory Transfer), Arithmetic Micro-Operations, Logic Micro-Operations, Shift Micro-Operations, Arithmetic logical shift unit	6	10
2	Basic Computer Organization and Design Instruction codes, Computer registers, computer instructions, Timing and Control, Instruction cycle, Memory-Reference Instructions, Input-output and interrupt, Complete computer description, Design of Basic computer, design of Accumulator Unit.	4	10
3	Programming The Basic Computer Introduction, Machine Language, Assembly Language, assembler, Program loops, Programming Arithmetic and logic operations, subroutines, I-O Programming.	4	10
4	Micro programmed Control: Control Memory, Address sequencing, Micro program Example, design of control Unit	3	5
5	Central Processing Unit Introduction, General Register Organization, Stack Organization, Instruction format, Addressing Modes, data transfer and manipulation,Program Control, Reduced Instruction Set Computer (RISC)	4	15
6	Pipeline And Vector Processing Flynn's taxonomy, Parallel Processing, Pipelining, Arithmetic Pipeline, Instruction, Pipeline, RISC Pipeline, Vector Processing, Array Processors	3	10

7	Computer Arithmetic Introduction, Addition and subtraction, Multiplication Algorithms (Booth Multiplication Algorithm), Division Algorithms, Floating Point Arithmetic operations, Decimal Arithmetic Unit.	4	10
8	Input-Output Organization Input-Output Interface, Asynchronous Data Transfer, Modes Of Transfer, Priority Interrupt, DMA, Input-Output Processor (IOP), CPUIOP Communication, Serial communication.	4	10
9	Memory Organization Memory Hierarchy, Main Memory, Auxiliary Memory, Associative Memory, Cache Memory, Virtual Memory.	2	10
10	Multipreocessors Characteristics of Multiprocessors, Interconnection Structures, Inter-processor Arbitration, Inter-processor Communication and Synchronization, Cache Coherence, Shared Memory Multiprocessors.	4	10

Suggested Specification table with Marks (Theory):

Distribution of Theory Marks				
R Level	U Level	A Level	N Level	E Level

Legends: R: Remembrance; U: Understanding; A: Application, N: Analyze and E: Evaluate and above Levels (Revised Bloom's Taxonomy)

Note: This specification table shall be treated as a general guideline for students and teachers. The actual distribution of marks in the question paper may vary slightly from above table.

Reference Books:

1. M. Morris Mano, Computer System Architecture, Pearson
2. Andrew S. Tanenbaum and Todd Austin, Structured Computer Organization, Sixth Edition, PHI
3. M. Murdocca & V. Heuring, Computer Architecture & Organization, WILEY
4. John Hayes, Computer Architecture and Organization, McGrawHill

Course Outcomes:

After successful completion of the course students should be able to:

1. To apply knowledge of the processor's internal registers and operations by use of a
2. PC based microprocessor simulator.
3. To write assembly language programs and download the machine code that will
4. provide solutions real-world control problems.
5. To eliminate or remove stall by altering order of instructions
6. To write programs using the capabilities of the stack, the program counter, the status register and show how these are used to execute a machine code program.

List of Tutorial:

1) A digital computer has a common bus system for 16 registers of 32 bits each. The bus is constructed with multiplexers.
   How many selection inputs are there in each multiplexer ?
   What size of multiplexers are needed ?
   How many multiplexers are there in the bus ?

2) The following transfer statements specify a memory. Explain the memory operation in each case.
   R2 ←M[AR]
   M[AR]←R3
   R5←M[R5]

3) The adder-subtractor circuit of Fig 4.7 has the following values for input mode M and data inputs A and B. In each case, determine the values of the outputs : S_3, S_2, S_1, S_0 and C_4.

	M	A	B
a.	0	0111	0110
b.	0	1000	1001
c.	1	1100	1000
d.	1	0101	1010
e.	1	0000	0001

4) Design a 4-bit combinational circuit decrementer using four full-adder circuits.

5) Design a digital circuit that performs the four logic operations of exclusive-OR, exclusive-NOR, NOR, and NAND. Use two selection variables. Show the logic diagram of one typical stage.

6) Register A holds the 8bit binary 11011001. Determine the B operand and the logic microoperation to be performed in order to change the value in A to :
   f. 01101101
   g. 11111101

7) The 8bit registers AR, BR, CR and DR initially have the following values :
   AR = 11110010
   BR = 11111111
   CR = 10111001
   DR = 11101010

8) Determine the 8bit values in each register after the execution of the following sequence of microoperations.

AR ←AR + BR
CR ←CR Λ DR, BR ← BR + 1
AR ← AR – CR

9) An output program resides in memory starting from address 2300. It is executed after the computer recognizes an interrupt when FGO becomes a 1 (while IEN = 1).
   a. What instruction must be placed at address 1 ?
   b. What must be the last two instruction of the output program ?

10) Write an assembly level program for the following pseudocode.
   SUM = 0
   SUM = SUM + A + B
   DIF = DIF – C
   SUM = SUM + DIF

11) Write a program loop using a pointer and a counter to clear the contents of hex locations 500 to 5FF with 0.

12) Write an ALP to add two Double-Precision numbers.

13) Write a program that evaluates the logic ex-or of two logic operands.

14) Write a program for the arithmetic shift-left operation. Branch to OVF if an overflow occurs.

15) For the given program below :
    1. Explain in words what the program accomplishes when it is executed. What is the value of location CTR when the computer halts ?
    2. List the address symbol table obtained during the first pass of the assembler.

```
        ORG 100
        CLE
        CLA
        STA CTR
        LDA WRD
        SZA
        BUN ROT
        BUN STP
ROT,    CIL
        SZE
        BUN AGN
        BUN ROT
AGN,    CLE
        ISZ CTR
        SZA
        BUN ROT
STP,    HLT
CTR,    HEX 0
WRD,    HEX 62C1
```

16) Write a subroutine to subtract two numbers. In the calling program, the BSA instruction is followed by the subtrahend and minuend. The difference is returned to the main program in the third location following the BSA instruction.

17) Convert the following into reverse polish notation.
    1) A+B*[C*D+E*(F+G)]
    2) A*[B+C*(D+E)] / [F+G*(H+I)]

18) Explain Stack and evaluate the following expression using stack
    (3+4)*[10(2+6)+8]

List of Open Source Software/learning website:

- NPTEL Lecture Series
- http://www.intel.com/pressroom/kits/quickreffam.htm
- web.stanford.edu/class/ee282/

ACTIVE LEARNING ASSIGNMENTS: Preparation of power-point slides, which include videos, animations, pictures, graphics for better understanding theory and practical work – The faculty will allocate chapters/ parts of chapters to groups of students so that the entire syllabus to be covered. The power-point slides should be put up on the web-site of the College/ Institute, along with the names of the students of the group, the name of the faculty, Department and College on the first slide. The best three works should submit to GTU.