GUJARAT TECHNOLOGICAL UNIVERSITY, AHMEDABAD, GUJARAT

COURSE CURRICULUM
COURSE TITLE: VLSI
(COURSE CODE: 3361104)

Diploma Programme in which this course is offered	Semester in which offered
Electronics and Communication Engineering	Sixth

1. RATIONALE

Digital integrated circuits are integral part of electronic equipment/gadgets starting from small toys to complex computer systems including personal digital assistants, mobile phones and Multimedia agents. This course will enable the students to acquire the basic skills to develop codes for VLSI circuits through VHDL programming. This course will also enable them to use FPGA and ASIC chips for design and development of various applications. Thus this course is an advance but very useful course for electronic engineers.

2. COMPETENCY

The course content should be taught and implemented with the aim to develop required skills in the students so that they are able to acquire following competency:

- **Develop codes through VHDL programming for VLSI based electronic systems**

3. COURSE OUTCOMES

The theory should be taught and practical should be undertaken in such a manner that students are able to acquire required learning outcomes in cognitive, psychomotor and affective domains to demonstrate the following course outcomes:

i. Maintain MOS based systems
ii. Maintain MOS inverters
iii. Maintain MOS circuits
iv. Develop VHDL Programs related to Combinational circuits
v. Develop VHDL Programs related to Sequential circuits

4. TEACHINGAND EXAMINATION SCHEME

Teaching Scheme (In Hours)			Total Credits (L+T+P)	Examination Scheme				
				Theory Marks		Practical Marks		Total Marks
L	**T**	**P**	**C**	**ESE**	**PA**	**ESE**	**PA**	
4	0	2	6	70	30	20	30	**150**

Legends: L- Lecture; **T-** Tutorial/Teacher Guided Student Activity; **P -** Practical; **C -**Credit; **ESE**-End Semester Examination; **PA** –Progressive Assessment

5. COURSE DETAILS

Unit	Major Learning Outcomes (in cognitive domain)	Topics and Sub-topics
Unit – I. Digital System and MOS Transistor	1a. Describe of design methodologies and detail of Y Chart.	1.1 VLSI design flow, Y chart, Practical design flow
	1b Describe different domain and Define different terms regarding design Hierarchy.	1.2 Design Hierarchy-Structural Decomposition in the physical (geometrical) domain
	1c Explain the types of FPGA Technology.	1.3 FPGA, Gate Array Design, Standard Cell Based Design, Full Custom Design
	1d Explain Energy Band Diagram and Structure of MOS	1.4 MOS structure
	1e Explain effect of external bias on two terminal MOS device with energy band diagram.	1.5 MOS system under external bias
	1f Explain Formation of channel with different symbols of MOSFET. 1g Explain gradual channel approximation.	1.6 Structure and operation of MOSFET transistor 1.7 MOSFET current- voltage Characteristics
Unit– II MOS Inverters	2a Explain the working of MOS Inverter	2.1 MOS Inverter : concept and working
	2b Explain operation of resistive load inverter without mathematical derivation of V_{OL}, V_{OH}, V_{IL},V_{IH}, $V_{TH.}$ (Write Only Final Equation).	2.2 Resistive load Inverter
	2c Describe inverter circuit with saturated and Linear Enhancement and Depletion type load. 2d Compare enhancement load NMOS and Depletion Load NMOS.	2.3 Inverter with n-type MOSFET Load, Enhancement load NMOS, Depletion Load NMOS 2.4 Enhancement load and Depletion Load NMOS
	2e Explain CMOS Inverter with Different Operating Modes of nMOS and pMOS transistor. 2f Describe the working of Cascaded stages	2.5 CMOS Inverter: Circuit operation and description 2.6 Cascaded CMOS Inverter stages
Unit– III MOS Circuits	3a Explain two input NAND and NOR Gate with depletion NMOS load.	3.1 Combinational MOS Logic Circuits.
	3b Explain Two input NAND and NOR Gate using CMOS logic.	3.2 CMOS logic circuits
	3c Differentiate AOI and OAI Logic. 3d Design simple XOR function.	3.3 Complex logic circuit
	3e Describe the working of SR latch circuit. 3f Distinguish Clocked latch and Flip-Flop circuit.	3.4 Sequential MOS circuit 3.5 VLSI Technology-Environment & Processes in brief

Unit	Major Learning Outcomes (in cognitive domain)	Topics and Sub-topics
Unit-IV Introduction to VHDL	4a Introduction to VHDL Programming methodology	4.1 Data flow, behavioural, structural
	4b Develop VHDL Programs related to basic logic gates.	4.2 Logic operations viz. AND,OR, NOR,NAND,NOT,EXOR, EXNOR etc.
	4c Develop VHDL Programs related to Fundamental Arithmetic operations.	4.3Adder and Subtractor.
Unit-V VHDL Programming	5a. Develop VHDL Programs related to Combinational circuits.	5.1 Combinational circuits- Multiplexer and De multiplexer, Decoder and Encoder. 5.2 4 bit Parallel Adder. 5.3 Parity Generator and parity checker.
	5b. Develop VHDL Programs related to Sequential circuits.	5.4 Basic sequential circuits- SR , D Latch, RS, T, JK Flip flop 5.5 Parallel input Parallel output Shift Register, Up Counter, Down Counter

6 SUGGESTED SPECIFICATION TABLE WITH HOURS and MARKS (Theory)

Unit	Unit Title	Teaching Hours	Distribution of Theory Marks			
			R Level	U Level	A Level	Total Marks
I	Digital System and MOS Transistor	8	4	6	6	16
II	MOS Inverters	12	4	4	6	14
III	MOS Circuits	12	5	5	8	18
IV	Introduction to VHDL	12	4	4	4	12
V	VHDL Programming	12	3	3	4	10
Total		**56**	**20**	**22**	**28**	**70**

Legends: **R** = Remember; **U** = Understand; **A** = Apply and above levels (Bloom's revised taxonomy)

Note: This specification table shall be treated as a general guideline for students and teachers. The actual distribution of marks in the question paper may vary slightly from above table.

7 SUGGESTED EXERCISES/PRACTICALS

The practical should be properly designed and implemented with an attempt to develop different types of skills **(outcomes in psychomotor and affective domain)** so that students are able to acquire the competencies/programme outcomes. Following is the list of practical exercises for guidance.

Note*: Here only outcomes in psychomotor domain are listed as practical. However, if these practical are completed appropriately, they would also lead to development of certain outcomes in affective domain which would in turn lead to development of* ***Course Outcomes***

*related to affective domain. Thus over all development of **Programme Outcomes (**as given in a common list at the beginning of curriculum document for this programme) would be assured. Faculty should refer to that common list and should ensure that students also acquire outcomes in affective domain which are required for overall achievement of Programme Outcomes/Course Outcomes.*

S. No.	Unit No.	Practical Exercises (Outcomes' in Psychomotor Domain)	Approx. Hours Required
1	IV	Identify VHDL entities and coding styles.	2
2	IV	Simulate the Basic logic gates using VHDL.	2
3	IV	Simulate the Universal logic gates using VHDL	2
4	IV	Simulate X-OR and X-NOR logic gates using VHDL	2
5	IV	Simulate Half Adder using VHDL	2
6	IV	Simulate Full Adder using VHDL	2
7	IV	Simulate Half Substracter using VHDL	2
8	IV	Simulate Full Substracter using VHDL	2
9	V	Simulate 4 : 1 mux using VHDL	2
10	V	Simulate 1 : 4 de-mux using VHDL	2
11	V	Simulate 3 : 8 decoder using VHDL	2
12	V	Simulate 8 : 3 encoder using VHDL	2
13	V	Simulate SR flip-flops using VHDL	2
14	V	Simulate D flip-flops using VHDL	2
15	V	Simulate JK flip-flops using VHDL	2
16	V	Simulate T flip-flops using VHDL	2
17	V	Simulate 4 bit parallel adder using VHDL	2
18	V	Simulate 4 bit Up counter using VHDL	2
19	V	Simulate 4 bit Down counter using VHDL	2
20	V	Simulate any three above listed programs using Structural coding method	2
21	V	Hardware implementation of all above listed program	2
Total Hours (perform any of the practical exercises for a total of minimum 28 hours from above list depending upon the availability of resources so that skills matching with the most of the outcomes in the every unit is included)			**42**

8 SUGGESTED STUDENT ACTIVITIES

Following is the list of proposed student activities like:

i. Survey Current requirement for Hardware/ Chip at your Company/ Department/ Institute.
ii. Identify basic Circuits etc.
iii. Project- Build a small ASIC for your Home /Community.
iv. Enhance features and components of your ASIC by providing more Hardware.
v. Visit industries where equipment/gadgets using VLSI are being manufactured/assembled.

9 SPECIAL INSTRUCTIONAL STRATEGIES (if any)

i. Show Video/ Animation film explaining VLSI Design which are available on internet.
ii. Arrange expert lecture on VHDL programming for real life applications.

10 SUGGESTED LEARNING RESOURCES

A) Books

S. No.	Title of Book	Author	Publication
1.	CMOS DIGITAL INTEGRATED CIRCUITS	Sung Mo Kang	TMH
2.	Introduction to VLSI Circuits and Systems.	Uyemura J.P.	WILEY INDIA PVT. LTD.
3.	VLSI DESIGN	Das Debaprasad	OXFORD
4.	VLSI DESIGN Theory and Practice	Vij Vikrant,Er. Syal Nidhi	LAXMI PUBLICATIONS PVT. LTD.
5.	Circuit design with VHDL	Pedroni V.A.	PHI
6.	VHDL Modelling of systems	Znawabi	TMH
7.	VHDL Programming by Example	Perry Douglas L.	MGH
8.	VHDL design	Bhaskar J	Pearson
9.	VLSI Technology	Chang C.Y. and Sze S. M.	McGraw Hill

B) Major Equipment/Instruments with Broad Specifications

i. Computer System
ii. VLSI Trainer Kits
iii. VHDL Simulator Software

C) Software/Learning Websites

i. QUARTUS-II-ALTERA EVAL VERSION
ii. ModelSim® HDL simulator for use by students in their academic coursework.
iii. ISE Simulator
iv. http://www.youtube.com/watch?v=9SnR3M3CIm4

11 COURSE CURRICULUM DEVELOPMENT COMMITTEE

Faculty Members from Polytechnics

- **Prof. K N Vaghela,** Sr. Lecturer in EC, Govt. Poly, Ahmedabad
- **Prof. U V Buch,** Sr. Lecturer in EC, Govt. Poly for Girls, Surat
- **Prof. J D Chauhan,** Lecturer in EC, Band B Poly, V. V. Nagar
- **Prof. L J Vora,** Lecturer in EC, Govt. Poly, Vadnagar

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- **Prof. Sanjeet Kumar**, Assistant Professor, Department of Electrical and Electronics Engineering**.**
- **Dr. Anjali Potnis**, Assistant Professor, Department of Electrical and Electronics Engineering