Course Name : Electronics Engineering Group

Course Code : EJ/ET/EX/EN/EV/ED/EI/IE

Semester : Sixth Semester for EJ/ET/EX/EN/EV/IE and Seventh for ED/EI

Subject Title : Very Large Scale Integration (Elective)

Subject Code : 17659

Teaching and Examination Scheme:

Teaching Scheme			Examination Scheme					
TH	TU	PR	PAPER HRS	TH	PR	OR	TW	TOTAL
03	--	02	03	100	--	--	25@	125

NOTE:

- **Two tests each of 25 marks to be conducted as per the schedule given by MSBTE.**
- **Total of tests marks for all theory subjects are to be converted out of 50 and to be entered in mark sheet under the head Sessional Work (SW).**

Rationale:

Very-Large-Scale Integration (**VLSI**) is the process of creating integrated circuits by combining thousands of transistors into a single chip. VLSI began in the 1970s when complex semiconductor and communication technologies were being developed. The microprocessor is a VLSI device. VLSI design is effective in providing potential engineers with exposure to both front-end and back-end processes. **Very-Large-Scale Integration is** an emerging technology trend in the industry. VLSI design and verification is done using the RTL Coding and verification tools.

VLSI design tools eventually included not only design entry and simulation but eventually cell-based routing, ROM compilers, and a state machine compiler. The tools were an integrated design solution for IC design and not just point tools, or more general purpose system tools.

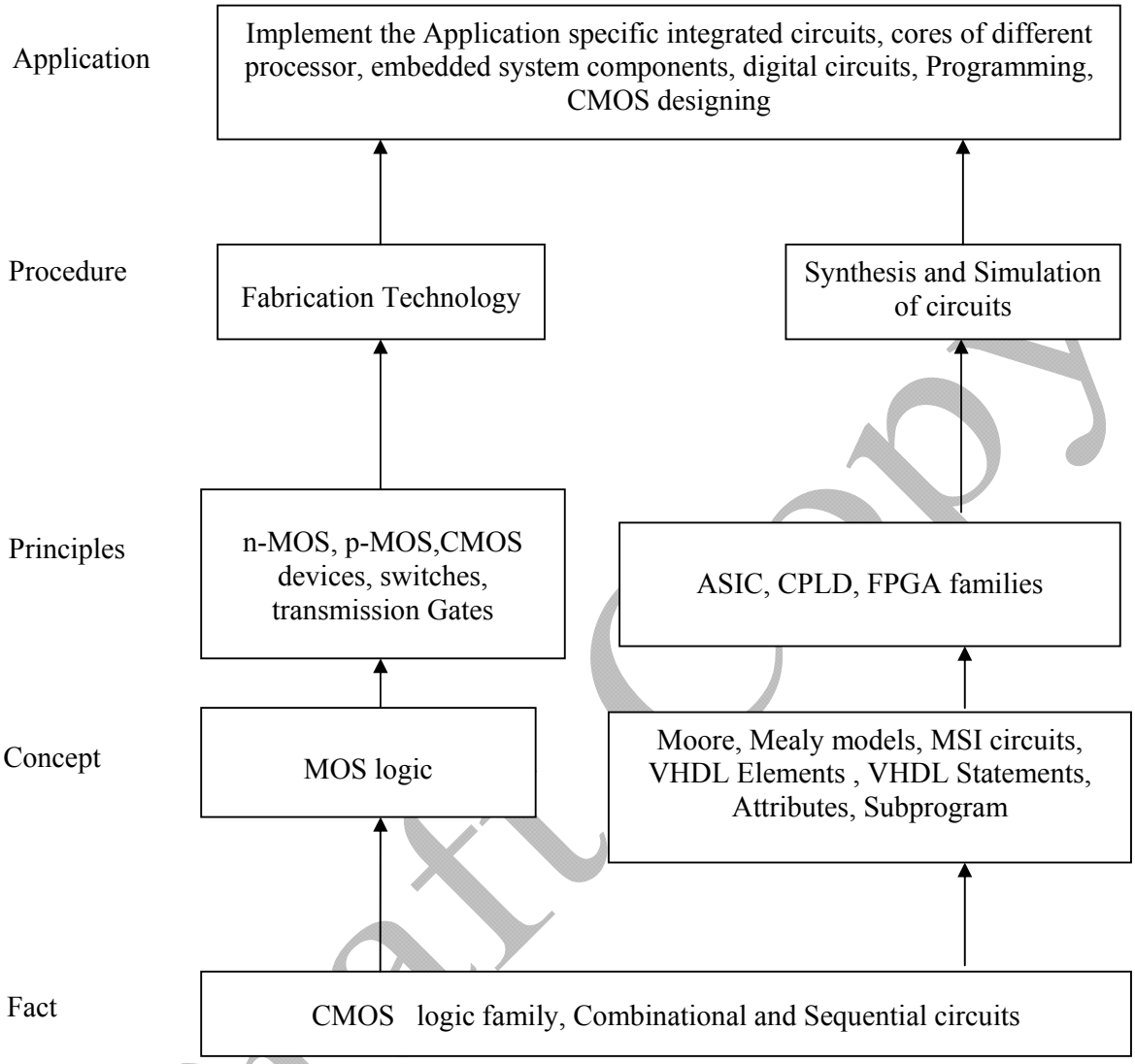
The VLSI is intended for the students having prerequisite of principles of analog and digital electronics. Students can use this knowledge in the digital design field to implement combinational and sequential logic circuit, ASIC, cores of various processors using HDL. They also design CMOS Logics at foundry levels. Students can utilize the basics of VLSI design tools as programmer, designers in IT, embedded systems in industrial sector.

General Objectives:

The student will be able to

1. Develop the state diagram, state table and built Moore and Mealy models
2. Implement logical equations using CMOS technology
3. Develop program to implement combinational and sequential logic circuit using VHDL and synthesize and optimum coding style.
4. Act as industry logic designers for imparting standard ICs, ASIC libraries**.**

Learning Structure:



Theory:

Topic and Contains	Hours	Marks
Topic 1: Introduction to Advanced Digital Design **Specific Objectives:** ➢ Develop the state diagram, state table ➢ Develop model of Moore and Mealy machine **Contents :** 1. Review of Sequential Logic : Asynchronous and Synchronous, Metastability, Noise margins, Power Fan-out, Skew (Definitions only) 2. Moore and Mealy Models, state machine notation, examples on Moore and mealy: counter, sequence detector only	04	14
Topic 2: Introduction to CMOS Technology ➢ Implement CMOS logic and logical equations. ➢ Comprehend CMOS processing Technology **Contents :** • Comparison of BJT and CMOS parameters • Design of Basic gates using CMOS: Inverter, NOR, NAND, MOS transistor switches, transmission gates. • Drawing of complex logic using CMOS (building of logic gate as per the Boolean equation of three variable) • Estimation of layout resistance and capacitance, switching characteristics, • Fabrication process: Overview of wafer processing, Oxidation, epitaxy, deposition, Ion–Implementation and diffusion, silicon gate process. • Basics of NMOS, PMOS and CMOS: nwell, pwell, twin tub process.	12	20
Topic 3: Introduction to VHDL ➢ Comprehend Hardware description language , its components and programming syntax **Contents :** • Introduction to HDL: History of VHDL, Pro's and Con's of VHDL • VHDL Flow elements of VHDL(Entity, Architecture, configuration, package, library only definitions) • Data Types, operators, operations • Signal, constant and variables(syntax and use)	08	14
Topic 4: VHDL Programming ➢ Develop program to implement combinational and sequential logic circuit using VHDL. **Contents :** • Concurrent constructs (when, with, process) • Sequential Constructs (process, if, case, loop, assert, wait) • Simple VHDL program to implement Flip Flop, Counter, shift register, MUX, DEMUX, ENCODER, DECODER, MOORE, MEALY machines • Test bench and its applications	08	16
Topic 5: HDL Simulation and Synthesis ➢ Comprehend VHDL simulation and synthesis. **Contents :** • Event scheduling, sensitivity list, zero modeling, simulation cycle,	12	20

comparison of software and hardware description language, • delta delay, Types of simulator event based and cycle based • HDL Design flow for synthesis • Efficient Coding Styles, Optimizing arithmetic expression, sharing of complex operator		
Topic 6: Introduction to ASIC, FPGA, PLD ➢ Comprehend ASIC, FPGA and PLDs. **Contents :** • ASIC design flow • CPLD -Xilinx and Atmel series architecture, Details of internal block diagram • Introduction to FPGA like Xilinx (FPGA), SPARTAN 3 series and Atmel	04	16
Total	**48**	**100**

Practical:

Intellectual Skills:

1. Use the different VLSI design Software tools for programming, simulation and synthesis.
2. Learn different Programmable logic devices (CPLD, FPGA, etc) and selection for target implementation

Motor Skills:

1. Write and test and debug the VHDL programming
2. Make the different connections for programming PLDs as a target device
3. Simulate and implement different programming modules on PLDs

List of Practical:

1. Write VHDL program for any two basic gates.
2. Write VHDL program for full adder / subtractor & Synthesize using FPGA
3. Write VHDL program for 8:1 multiplexer & Synthesize using FPGA
4. Write VHDL program for 2:4 Decoder & Synthesize using FPGA
5. Write VHDL program for 8:3 Encoder & Synthesize using FPGA
6. Write VHDL program for synchronous counter & Synthesize using FPGA
7. Write VHDL program for binary to gray code converter & synthesize using FPGA
8. Interfacing of DAC and ADC using FPGA
9. Interfacing Stepper motor controller using FPGA
10. Implement four Bit ALU or sequence generator.

Learning Resources:
Books:

Sr. No.	Author	Title	Publisher
1	Gaganpreet Kaur	VHDL Basics to programming	Pearson
2	John M. Yarbrough	Digital Logic: Application and design	Thomson
3	William I. Fletcher	An Engineering approach to digital design	Prentice-Hall of India
4	Neil H. E. Weste Kamran Eshraghian	Principals Of CMOS VLSI Design: A Systems Perspective	Pearson Education
5	Douglas Perry	VHDL Programming by example	Tata McGraw-Hill
6	Sarkar & Sarkar	VLSI design and EDA tools	Scitech Publication India Ltd

Web Sites:

www.xilinx.com
www.altera.com