Course Code	Course Name	Teaching Scheme			Credits Assigned			
		Theory	Practical	Tutorial	Theory	TW/Practical	Tutorial	Total
ETC606	VLSI Design	04	--	--	04	--	--	04

Course Code	Course Name	Examination Scheme							
		Theory Marks				Term Work	Practical	Oral	Total
		Internal assessment			End Sem. Exam				
		Test 1	Test 2	Avg. of Test 1 and Test 2					
ETC606	VLSI Design	20	20	20	80	--	--	--	100

Course Pre-requisite:

- ETC303: Digital Electronics
- ETC302: Analog Electronics-I
- ETC402: Analog Electronics-II
- ETC505: Integrated Circuits

Course Objectives:

- To teach fundamentals of VLSI circuit design and implementation using circuit simulators and layout editors.
- To highlight the circuit design issues in the context of VLSI technology.

Course Outcomes: After successful completion of the course student will be able to

- Demonstrate a clear understanding of CMOS fabrication flow and technology scaling.
- Design MOSFET based logic circuit
- Draw layout of a given logic circuit
- Realize logic circuits with different design styles
- Demonstrate an understanding of working principle of operation of different types of memories
- Demonstrate an understanding of working principles of clocking, power reduction and distribution

Module No.		Topics	Hrs.
1		**MOSFET Fabrication and Scaling**	08
	1.1	**Fabrication:** Fabrication process flow for NMOS and CMOS, CMOS Latch-up	
	1.2	**MOSFET Scaling:** Types of scaling, short channel effects, Level 1 and Level 2 MOSFET Models	
	1.3	**Layout:** Lambda based design rules, MOSFET capacitances	
2		**MOSFET Inverters**	10
	2.1	**Circuit Analysis:** Static and dynamic analysis (Noise, propagation delay and power dissipation) of resistive load and CMOS inverter. Comparison of all types of MOS inverters. Design of CMOS inverters and its layout.	
	2.2	**Logic Circuit Design:** Analysis and design of 2-I/P NAND and NOR using equivalent CMOS inverter.	
3		**MOS Circuit Design Styles**	10
	3.1	**Design Styles:** Static CMOS, Pass Transistor Logic, Transmission Gate, Pseudo NMOS, Domino, NORA, Zipper, C^2MOS	
	3.2	**Circuit Realization:** SR Latch, JK FF, D FF, 1 Bit Shift Register, MUX, Decoder using above design styles and their layouts	
4		**Semiconductor Memories**	08
	4.1	**SRAM:** ROM Array, SRAM (operation, design strategy, leakage currents, read/write circuits), DRAM (Operation 3T, 1T, operation modes, leakage currents, refresh operation, Input-Output circuits), Flash (mechanism, NOR flash, NAND flash), layout of SRAM and DRAM	
	4.2	**Peripheral Circuits:** Sense Amplifier, Decoder	
5		**Data Path Design**	08
	5.1	**Adder:** Bit adder circuits, Ripple carry adder, CLA adder	
	5.2	**Multipliers and shifter:** Partial-product generation, partial-product accumulation, final addition, Barrel Shifter	
6		**VLSI Clocking and System design**	08
	6.1	**Clocking:** CMOS clocking styles, Clock generation, stabilization and distribution	
	6.2	**Low Power CMOS Circuits:** Various components of power dissipation in CMOS, Limits on low power design, low power design through voltage scaling.	
	6.3	**IO pads and Power Distribution:** ESD protection, Input circuits, Output circuits, Simultaneous switching noise, power distribution scheme	
	6.4	**Interconnect:** Interconnect delay model, interconnect scaling and crosstalk	
Total			52

Recommended Books:

1. Sung-Mo Kang and Yusuf Leblebici, "*CMOS Digital Integrated Circuits Analysis and Design*", Tata McGraw Hill, 3rd Edition, 2012.
2. Jan M. Rabaey, Anantha Chandrakasan and Borivoje Nikolic, "*Digital Integrated Circuits: A Design Perspective*", Pearson Education, 2nd Edition.
3. John P. Uyemura, "*Introduction to VLSI Circuits and Systems*", Wiley, Student Edition, 2013.
4. Neil H. E. Weste, David Harris and Ayan Banerjee, "*CMOS VLSI Design: A Circuits and Systems Perspective*", Pearson Education, 3rd Edition.
5. R. Jacob Baker, "*CMOS Circuit Design, Layout and Simulation*", Wiley, 2nd Edition, 2013

Internal Assessment (IA):
Two tests must be conducted which should cover at least 80% of syllabus. The average marks of two tests should be considered as final IA marks

End Semester Examination:
1. Question paper will comprise of 6 questions, each of 20 marks.
2. Total 4 questions need to be solved.
3. Question No.1 will be compulsory and based on entire syllabus wherein sub questions for 2 to 5 marks will be asked.
4. Remaining questions will be selected from all the modules.