Subject Code	Subject Name	Teaching Scheme			Credits Assigned			
		Theory	Pract.	Tut.	Theory	TW/Pract.	Tut.	Total
EXC303	Digital Circuits and Design	04	--	-	04	--	-	04

Sub. Cod	Subject Name	Examination Scheme							
		Theory Marks				TW	Pract.	Oral	Total
		Internal Assessment			End Semester Exam				
EXC303	Digital Circuits and Design	Test 1	Test 2	Average of Test1 & Test2					
		20	20	20	80	--	-	--	100

Prerequisite: FEC105 Basic Electrical & Electronics Engineering

Course Objectives:

1. To deliver the knowledge, motivate and train students in logic design
2. To introduce the students to various logic gates, SOP, POS and their minimization techniques.
3. To explain and describe various logic families and to provide information on different IC's.
4. To teach the working of combinational circuits and their applications.
5. To make students aware of characteristics of various types of SSI, LSI and MSI devices and their use in various applications.
6. To teach students to analyze, understand and design sequential circuits.
7. To describe State Machines and explain their design using state diagrams.
8. To explain various types of programmable devices
9. To train students in writing program with hardware description languages.
10. To prepare students for understanding courses like microprocessors, microcontrollers, VLSI design, embedded systems and digital communications

Course Outcome:

1. Ability to develop a logic and apply it to solve real life problems
2. Ability to understand current applications, trends and new directions in logic design
3. Ability to reduce SOP and POS equations.
4. Ability to understand differences between logic families TTL and CMOS
5. Ability to understand various SSI, LSI and MSI devices
6. Ability to use SSI, LSI and MSI devices in various applications
7. Ability to analyze, design and implement combinational circuits
8. Ability to analyze, design and implement sequential circuits
9. Ability to solve state machines
10. Ability to design state machines using state diagrams, State Reduction techniques and State machine synthesis using transition lists
11. Ability to understand the concept of simulation, synthesis and implementation
12. Ability to use hardware description languages for logic circuit design.
13. Ability to understand programmable logic devices
14. Ability to program CPLD and FPGA

Module No.	Topics	Hrs.
1.0	**Fundamentals of Digital Design**	**14**
1.1	**Logic Gates:** Review of basic gates, Universal gates, Sum of products and products of sum, minimization with Karnaugh Map (upto four variables) and realization.	
1.2	**Logic Families:** Types of logic families (TTL and CMOS), characteristic parameters (propagation delays, power dissipation, Noise Margin, Fan-out and Fan-in), transfer characteristics of TTL NAND, Interfacing CMOS to TTL and TTL to CMOS.	
1.3	**Combinational Circuits using basic gates as well as MSI devices:** Half adder, Full adder, Half Subtractor, Full Subtractor, multiplexer, demultiplexer, decoder, Comparator (Multiplexer and demultiplexer gate level upto 4:1). MSI devices IC7483, IC74151, IC74138, IC7485.	
2.0	**Elements of Sequential Logic Design :**	**10**
2.1	**Sequential Logic:** Latches and Flip-Flops (Conversions, timing considerations and metastability are **not** expected)	
2.2	**Counters:** Asynchronous, Synchronous Counters, Up Down Counters, Mod Counters, Ring Counters Shift Registers, Universal Shift Register	
3.0	**Sequential Logic Design:**	**10**
3.1	Mealy and Moore Machines, Clocked synchronous state machine analysis, State reduction techniques and state assignment, Clocked synchronous state machine design. (*Complex word problems like traffic light controller etc. are not expected*)	
3.2	MSI counters (7490, 74163, 74169) and applications, MSI Shift registers (74194) and their applications	
4.0	**Programmable Logic Devices:**	**07**
4.1	Concepts of PAL and PLA. Simple logic implementation using PAL and PLA. Introduction to CPLD and FPGA architectures.	
5.0	**Simulation:**	**07**
5.1	Functional Simulation, Timing simulation, Logic Synthesis, RTL	
5.2	Introduction to VHDL, Framework of VHDL Program.	
6.0	**Testability:**	**06**
6.1	Fault Models, Stuck at faults, Bridging faults, Controllability and Observability	
6.2	Path sensitization, ATPG, Design for Testability, Boundary Scan Logic, JTAG and Built in self test.	
	Total	**52**

Recommended Books

1. William I. Fletcher, 'An Engineering Approach to Digital Design', PHI.
2. B. Holdsworth and R. C. Woods, 'Digital Logic Design', Newnes, 4th Edition
3. Morris Mano, Digital Design, Pearson Education, Asia 2002.
4. John F. Wakerley, Digital Design Principles And Practices, third Edition Updated, Pearson Education, Singapore, 2002
5. Anil K. Maini, Digital Electronics, Principles, Devices and Applications, Wiley
6. Stephen Brown and Zvonko Vranesic, Fundamentals of digital logic design with VHDL, McGraw Hill, 2nd Edition.

Internal Assessment (IA):

Two tests must be conducted which should cover at least 80% of syllabus. The average marks of both the test will be considered as final IA marks

End Semester Examination:

1. Question paper will comprise of 6 questions, each carrying 20 marks.

2. The students need to solve total 4 questions.
3: Question No.1 will be compulsory and based on entire syllabus. 4:
Remaining question (Q.2 to Q.6) will be set from all the modules. 5:
Weightage of marks will be as per Blueprint.