| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| **Total** | | **110** | **110** | **110** | **440** | **100** | **50** | **50** | **750** |

| Subject Code | Subject Name | Teaching Scheme | | | Credits Assigned | | | |
|---|---|---|---|---|---|---|---|---|
| | | Theory | Practical | Tutorial | Theory | Practical | Tutorial | Total |
| **EXC601** | **Basic VLSI Design** | **04** | **--** | **--** | **04** | **--** | **--** | **04** |

| Subject Code | Subject Name | Examination Scheme | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | Theory Marks | | | | Term Work | Practical | Oral | Total |
| | | Internal assessment | | | End Sem. Exam | | | | |
| | | Test 1 | Test 2 | Avg. of Test 1 and Test 2 | | | | | |
| **EXC601** | **Basic VLSI Design** | **20** | **20** | **20** | **80** | **--** | **--** | **--** | **100** |

**Course Pre-requisite:**

- EXC302: Electronic Devices
- EXC303: Digital Circuits and Design
- EXC402: Discrete Electronic Circuits
- EXC502: Design With Linear Integrated Circuits

**Course Objectives:**

1. To teach fundamental principles of VLSI circuit design and layout techniques
2. To highlight the circuit design issues in the context of VLSI technology

**Course Outcomes:**

**After successful completion of the course student will be able to**

1. demonstrate a clear understanding of choice of technology and technology scaling
2. design MOS based circuits and draw layout
3. realize logic circuits with different design styles
4. demonstrate a clear understanding of system level design issues such as protection, timing and power dissipation

| Module No. | Unit No. | Topics | Hrs. |
|---|---|---|---|
| 1 | | **Technology Trend** | 6 |
| | 1.1 | **Technology Comparison:** Comparison of BJT, NMOS and CMOS technology | |
| | 1.2 | **MOSFET Scaling:** Types of scaling, Level 1 and Level 2 MOSFET Models, MOSFET capacitances | |
| 2 | | **MOSFET Inverters** | 10 |
| | 2.1 | **Circuit Analysis:** Static and dynamic analysis (Noise, propagation delay and power dissipation) of resistive load and CMOS inverter, comparison of all types of MOS inverters, design of CMOS inverters, CMOS Latch-up | |
| | 2.2 | **Logic Circuit Design:** Analysis and design of 2-I/P NAND and NOR using equivalent CMOS inverter | |
| 3 | | **MOS Circuit Design Styles** | 10 |
| | 3.1 | **Design Styles:** Static CMOS, pass transistor logic, transmission gate, Pseudo NMOS, Domino, NORA, Zipper, $C^2$MOS, sizing using logical effort | |
| | 3.2 | **Circuit Realization:** SR Latch, JK FF, D FF, 1 Bit Shift Register, MUX, decoder using above design styles | |
| 4 | | **Semiconductor Memories** | 08 |
| | 4.1 | **SRAM:** ROM Array, SRAM (operation, design strategy, leakage currents, read/write circuits), DRAM (Operation 3T, 1T, operation modes, leakage currents, refresh operation, Input-Output circuits), Flash (mechanism, NOR flash, NAND flash) | |
| | 4.2 | **Peripheral Circuits:** Sense amplifier, decoder | |
| 5 | | **Data Path Design** | 08 |
| | 5.1 | **Adder:** Bit adder circuits, ripple carry adder, CLA adder | |
| | 5.2 | **Multipliers and shifter:** Partial-product generation, partial-product accumulation, final addition, barrel shifter | |
| 6 | | **VLSI Clocking and System Design** | 10 |
| | 6.1 | **Clocking:** CMOS clocking styles, Clock generation, stabilization and distribution | |
| | 6.2 | **Low Power CMOS Circuits:** Various components of power dissipation in CMOS, Limits on low power design, low power design through voltage scaling | |
| | 6.3 | **IO pads and Power Distribution:** ESD protection, input circuits, output circuits, simultaneous switching noise, power distribution scheme | |
| | 6.4 | **Interconnect:** Interconnect delay model, interconnect scaling and crosstalk | |
| | | **Total** | 52 |

**Recommended Books:**


1. Sung-Mo Kang and Yusuf Leblebici, "*CMOS Digital Integrated Circuits Analysis and Design*", Tata McGraw Hill, 3rd Edition.
2. Jan M. Rabaey, Anantha Chandrakasan and Borivoje Nikolic, "*Digital Integrated Circuits: A Design Perspective*", Pearson Education, 2nd Edition.
3. Etienne Sicard and Sonia Delmas Bendhia, "*Basics of CMOS Cell Design*", Tata McGraw Hill, First Edition.
4. Neil H. E. Weste, David Harris and Ayan Banerjee, "*CMOS VLSI Design: A Circuits and Systems Perspective*", Pearson Education, 3rd Edition.
5. Debaprasad Das, "*VLSI Design*", Oxford, 1st Edition.
6. Kaushik Roy and Sharat C. Prasad, "*Low-Power CMOS VLSI Circuit Design*", Wiley, Student Edition.


**Internal Assessment (IA):**

Two tests must be conducted which should cover at least 80% of syllabus. The average marks of both the tests will be considered as final IA marks

**End Semester Examination**:

1. Question paper will comprise of 6 questions, each carrying 20 marks.
2. Total 4 questions need to be solved.
3: Question No.1 will be compulsory and based on entire syllabus wherein sub questions of 2 to 5 marks will be asked.
4: Remaining questions will be selected from all the modules.

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