Subject Code	Subject Name	Teaching Scheme			Credits Assigned			
		Theory	Practical	Tutorial	Theory	Practical	Tutorial	Total
EXC603	Computer Organization	04	--	--	04	--	--	04

Subject Code	Subject Name	Examination Scheme							
		Theory Marks				Term Work	Practical	Oral	Total
		Internal assessment			End Sem. Exam				
		Test 1	Test 2	Avg. of Test 1 and Test 2					
EXC603	Computer Organization	20	20	20	80	--	--	--	100

Course objectives:
1. To conceptualize the basics of organizational and architectural issues of a digital computer.
2. To analyze performance issues in processor and memory design of a digital computer.
3. To understand various data transfer techniques in digital computer.
4. To analyze processor performance improvement using instruction level parallelism.

Course Outcomes:
The student should be able:
1. To understand basic structure of computer.
2. To perform computer arithmetic operations.
3. To understand control unit operations.
4. To understand the concept of cache mapping techniques.
6. To design memory organization (banks for different word size operations).
5. To understand the concept of I/O organization.
6. To conceptualize instruction level parallelism.

Module No.	Unit No.	Topics	Hrs.
1		**Introduction to Computer Organization**	**10**
	1.1	Fundamental units of computer organization, evolution of computers, von neumann model, performance measure of computer architecture	
	1.2	Introduction to buses and connecting I/O devices to CPU and Memory, bus structure,	
	1.3	Introduction to number representation methods, integer data computation, floating point arithmetic.	
2		**Processor Organization and Architecture**	**14**
	2.1	CPU Architecture, register organization, instruction formats, basic instruction cycle, instruction interpretation and sequencing	
	2.2	**Control unit:** soft wired (micro-programmed) and hardwired control unit design methods	
	2.3	Microinstruction sequencing and execution, micro operations, concepts of nano programming.	
	2.4	Introduction to RISC and CISC architectures and design issues, case study on 8085 microprocessor, features, architecture, pin configuration and addressing modes	
3		**Memory Organization**	**12**
	3.1	Introduction to memory and memory parameters, classifications of primary and secondary memories, types of RAM and ROM, allocation policies, memory hierarchy and characteristics	
	3.2	Cache memory concept, architecture (L1, L2, L3), mapping techniques, cache coherency	
	3.3	Interleaved and associative memory, virtual memory, concept, segmentation and paging, page replacement policies	
4		**Input / Output Organization**	**8**
	4.1	Types of I/O devices and access methods, types of buses and bus arbitration, I/O interface, serial and parallel ports	
	4.2	Types of data transfer techniques, programmed I/O, interrupt driven I/O and DMA	
	4.3	Introduction to peripheral devices, scanner, plotter, joysticks, touch pad, storage devices	
5		**Introduction To Parallel Processing System**	**4**
	5.1	Introduction to parallel processing concepts, Flynn's classifications, pipeline processing, instruction pipelining, pipeline stages, pipeline hazards	
6		**Introduction to Intel IA32 Architecture**.	**4**
	6.1	Intel IA32 family architecture, register structure, addressing modes, advancements in arithmetic and logical instructions, exception handling in IA32 architecture	
		Total	**52**

Recommended Books:
1. Carl Hamacher, Zvonko Vranesic and Safwat Zaky, "*Computer Organization*", Fifth Edition, Tata McGraw-Hill.
2. John P. Hayes, "*Computer Architecture and Organization*", Third Edition.
3. William Stallings, "*Computer Organization and Architecture: Designing for Performance*", Eighth Edition, Pearson.
4. B. Govindarajulu, "*Computer Architecture and Organization: Design Principles and Applications*", Second Edition, Tata McGraw-Hill.
1. Dr. M. Usha and T. S. Srikanth, "*Computer System Architecture and Organization*", First Edition, Wiley-India.
2. Ramesh Gaonkar, "*Microprocessor Architecture, Programming and Applications with the 8085"*, Fifth Edition,Penram.

Internal Assessment (IA):
Two tests must be conducted which should cover at least 80% of syllabus. The average marks of both the tests will be considered as final IA marks

End Semester Examination:
1. Question paper will comprise of 6 questions, each carrying 20 marks.
2. Total 4 questions need to be solved.
3: Question No.1 will be compulsory and based on entire syllabus wherein sub questions of 2 to 5 marks will be asked.
4: Remaining questions will be selected from all the modules.

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