Subject Code	Subject Name	Teaching Scheme (Hrs.)			Credits Assigned			
		Theory	Practical	Tutorial	Theory	Practical	Tutorial	Total
EXC 605	Digital Signal Processing and Processors	4	--	--	4	--	--	04

Subject Code	Subject Name	Examination Scheme							
		Theory Marks				Term Work	Practical	Oral	Total
		Internal assessment			End Sem. Exam				
		Test 1	Test 2	Ave. Of Test 1 and Test 2					
EXC 605	Digital Signal Processing and Processors	20	20	20	80	--	--	--	100

Course Objective:

1. To study DFT and its computation
2. To study the design techniques for digital filters
3. To study the finite word length effects in signal processing
4. To study the fundamentals of digital signal processors
5. To get acquainted with the DSP applications

Course Outcome:

Students will be able to understand concept of digital filters

1. Students will be able to decide the selection and design of digital filters
2. Students will understand the effect of hardware limitation
3. Students will be understand need of DSP processors
4. Students will be able to understand the use and application of DSP processors

Module No.	Unit No.	Topics	Hrs.
1.0		**Discrete Fourier Transform and Fast Fourier Transform**	10
	1.1	**Discrete Fourier Series**: Properties of discrete Fourier series, DFS representation of periodic sequences.	
	1.2	**Discrete Fourier transforms**: Properties of DFT, linear convolution of sequences using DFT, computation of DFT, relation between Z-transform and DFS	
	1.3	**Fast Fourier Transforms**: Fast Fourier transforms (FFT), Radix-2 decimation in time and decimation in frequency FFT algorithms, inverse FFT, and composite FFT	
2.0		**IIR Digital Filters**	10
	2.1	Mapping of S-plane to Z-plane, impulse invariance method, bilinear Z transformation (BLT) method, frequency warping, pre-warping	
	2.2	**Analog filter approximations**: Butter worth and Chebyshev, design of IIR digital filters from analog filters, design examples	
	2.3	Analog and digital frequency transformations	
3.0		**FIR Digital Filters**	10
	3.1	Characteristics of FIR digital filters, frequency response, location of the zeros of linear phase FIR filters	
	3.2	Design of FIR digital filters using window techniques, Gibbs phenomenon, frequency sampling technique, comparison of IIR and FIR filters	
4.0		**Finite Word Length Effects in Digital Filters**	08
	4.1	Number representation, fixed point, sign-magnitude, one's complement, two's complement forms, floating point numbers	
	4.2	Quantization, truncation, rounding, effects due to truncation and rounding, Input quantization error, Product quantization error, co-efficient quantization error, zero-input limit cycle oscillations, overflow limit cycle oscillations, scaling	
	4.3	Quantization in Floating Point realization IIR digital filters, finite word length effects in FIR digital filters, quantization effects in the computation of the DFT- quantization errors in FFT algorithms	
5.0		**Introduction to DSP Processors**	08
	5.1	Introduction to fixed point and floating point DSP processor, multiplier and multiplier accumulator (MAC), modified bus structures and memory access schemes in DSPs, multiple access memory, multiport memory, VLIW architecture, pipelining, special addressing modes, on-chip peripherals	
	5.2	Features of TMS 320c67xx DSP processor, architecture of TMS 320c67xx DSP processor, architecture features: computational units, bus architecture memory, data addressing, address generation unit, program control, program sequencer, pipelining, interrupts, features of external interfacing, on-chip peripherals, hardware timers, host interface port, clock generators, SPORT	
6.0		**Applications of DSP Processors**	06
	6.1	Speech Processing: Speech analysis, speech coding, sub band coding, channel vocoder, homomorphic vocoder, digital processing of audio signals.	
	6.2	**Radar signal processing**: Radar principles, radar system and parameter considerations, signal design	
Total			52

Recommended Books:

1. Proakis J., Manolakis D., "*Digital Signal Processing*", 4th Edition, Pearson Education
2. Oppenheim A., Schafer R., Buck J., "*Discrete Time Signal Processing*", 2nd Edition, Pearson Education.
3. Babu R., "*Digital Signal Processing*", 4th Edition, Scitech Publications.
4. B. Venkata Ramani and M. Bhaskar, "*Digital Signal Processors, Architecture, Programming and Applications*", Tata McGraw Hill, 2004.
5. L. R. Rabiner and B. Gold, "*Theory and Applications of Digital Signal Processing*", Prentice-Hall of India, 2006.
6. B. Kumar, "*Digital Signal Processing*", New Age International Publishers, 2014.

Internal Assessment (IA):

Two tests must be conducted which should cover at least 80% of syllabus. The average marks of both the tests will be considered as final IA marks

End Semester Examination:

1. Question paper will comprise of 6 questions, each carrying 20 marks.
2. Total 4 questions need to be solved.
3: Question No.1 will be compulsory and based on entire syllabus wherein sub questions of 2 to 5 marks will be asked.
4: Remaining questions will be selected from all the modules.

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