Subject Code	Subject Name	Teaching Scheme			Credits Assigned				
		Theory	Practical	Tutorial	Theory	TW/Practical	Tutorial	Total	
EXC702	IC	04			04			04	
	Technology								

Subject	Subject	Examination Scheme								
Code	Name	Theory Mark			ks	Term	Practical	Oral	Total	
		Internal assessment			End Sem.	Work				
		Test	Test	Avg. of	Exam					
		1	2	Test 1 and						
				Test 2						
EXC702	IC	20	20	20	80				100	
	Technology									

Course Pre-requisite:

- EXC302: Electronic Devices
- EXC303: Digital Circuits and Design
- EXC402: Discrete Electronic Circuits
- EXC502: Design With Linear Integrated Circuits
- EXC601: VLSI Design

Course Objectives:

- 1. To teach fundamental principles of fabrication of VLSI devices and circuits
- 2. To disseminate knowledge about novel VLSI devices

Course Outcomes:

After successful completion of the course student will be able to

- 1. demonstrate a clear understanding of CMOS fabrication flow and technology scaling
- 2. demonstrate a clear understanding of various MOS fabrication processes, semiconductor measurements, packaging, testing and advanced semiconductor technologies
- 3. discuss physical mechanism in novel devices
- 4. verify processes and device characteristics via simulations

1.0 Environment and Crystal Growth for VLSI Technology 8 1.1 Environment: Semiconductor technology trend, Clean rooms, Wafer cleaning 8 1.2 Semiconductor Substrate: Phase diagram and solid solubility, Crystal structure, Crystal defects, Czochralski growth, Bridgman growth of GaAs, Float Zone growth, Wafer Preparation and specifications 10 2.0 Fabrication Processes Part 1 10 2.1 Epitaxy: Molecular Beam Epitaxy, Vapor Phase Epitaxy, Liquid Phase Epitaxy, Evaluation of epitaxial layers 10 2.3 Silicon Oxidation: Thermal oxidation process, Kinetics of growth, Properties of Silicon Dioxide, Oxide Quality, high × and low × dielectrics 10 2.4 Diffusion: Nature of diffusion systems, problems in diffusion equation of diffused layers 10 3.0 Fabrication Processes Part 2 10 3.1 Etching: Wet chemical etching, dry physical etching, dry chemical etching, reactive ion etching, ion beam techniques 10 3.2 Lithography: Photoreactive materials, Pattern generation and make making, pattern transfer, Electron beam, Ion beam and X-ray lithography 33 3.4 CMOS Process Flow: N well, P-well and Twin tub 3.5 Design rules, Layout of MOS based circuits (gates and combinational logic), Buried and Buting Contact 10 4.0 <	Module No.	Unit No.	Topics	Hrs.			
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6.3 Graphene Device: Carbon nanotube transistor fabrication, CNT applications			important features)				
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Total 52		6.3		52			

Recommended Books:

- 1. James D. Plummer, Michael D. Deal and Peter B. Griffin, "Silicon VLSI Technology", Pearson, Indian Edition.
- 2. Stephen A. Campbell, "*The Science and Engineering of Microelectronic Fabrication*", Oxford University Press, 2nd Edition.
- 3. Sorab K. Gandhi, "VLSI Fabrication Principles", Wiley, Student Edition.
- 4. G. S. May and S. M. Sze, "Fundamentals of Semiconductor Fabrication", Wiley, First Edition.
- 5. Kerry Bernstein and N. J. Rohrer, "SOI Circuit Design Concepts", Kluwer Academic Publishers, 1st edition.
- 6. Jean-Pierre Colinge, "FinFETs and Other Multigate Transistors", Springer, 1st edition
- 7. M. S. Tyagi, "Introduction to Semiconductor Materials and Devices", John Wiley and Sons, 1st edition.
- 8. James E. Morris and Krzysztol Iniewski, "Nanoelectronic Device Applications Handbook", CRC Press
- 9. Glenn R. Blackwell, "The electronic packaging", CRC Press
- 10. Michael L. Bushnell and Vishwani D. Agrawal, "Essentials of Electronic Testing for digital, memory and mixed-signal VLSI circuits", Springer

Internal Assessment (IA):

Two tests must be conducted which should cover at least 80% of syllabus. The average marks of both the test will be considered as final IA marks

End Semester Examination:

- 1. Question paper will comprise of 6 questions, each of 20 marks.
- 2. Total 4 questions need to be solved.
- 3. Question No.1 will be compulsory and based on entire syllabus wherein sub questions of 2 to 5 marks will be asked.
- 4. Remaining question will be selected from all the modules.