Subject Code	Subject Name	Teaching Scheme			Credits Assigned			
		Theory	Practical	Tutorial	Theory	TW/Practical	Tutorial	Total
EXC801	CMOS VLSI Design	04	--	--	04	--	--	04

Subject Code	Subject Name	Examination Scheme							
		Theory Marks				Term Work	Practical	Oral	Total
		Internal assessment			End Sem. Exam				
		Test 1	Test 2	Avg. of Test 1 and Test 2					
EXC801	CMOS VLSI Design	20	20	20	80	--	--	--	100

Course Pre-requisite:

- EXC302: Electronic Devices
- EXC303: Digital Circuits and Design
- EXC402: Discrete Electronic Circuits
- EXC502: Design With Linear Integrated Circuits
- EXC601: VLSI Design
- EXC702: IC Technology

Course Objectives:

1. To teach analysis and design of building blocks of CMOS Analog VLSI Circuits.
2. To highlight the issues associated with the CMOS analog VLSI circuit design.

Course Outcomes:

After successful completion of the course student will be able to

1. discuss tradeoffs involved in analog VLSI Circuits.
2. analyze building blocks of CMOS analog VLSI circuits.
3. design building blocks of CMOS analog VLSI circuits
4. carry out verifications of issues involved in analog circuits via simulations

Module No.	Unit No.	Topics	Hrs.
1. 0		**CMOS analog building blocks**	8
	1.1	**MOS Models:** Necessity of CMOS analog design, Review of characteristics of MOS device, MOS small signal model, MOS spice models	
	1.2	**Passive and Active Current Mirrors:** Basic current mirrors, Cascode current mirrors and Active current mirrors	
	1.3	**Band Gap References:** General Considerations, Supply-independent biasing, Temperature independent references, PTAT current generation and Constant Gm biasing	
2.0		**Single Stage Amplifiers**	10
	2.1	**Configurations:** Basic concepts, Common source stage, Source follower, Common gate stage, Cascode stage	
	2.2	**Frequency Response and Noise:** General considerations, Common-source stage, Source followers, Common-gate stage, Cascode stage and Noise in single stage amplifiers	
3.0		**Differential Amplifiers**	10
	3.1	**Configurations:** Single ended and differential operation, Basic differential pair, Common-mode response, Differential pair with MOS loads, Gilbert cell	
	3.2	Frequency response and noise in differential pair	
4.0		**MOS Operational Amplifiers**	10
	4.1	**Op-amp Design:** General Considerations, performance parameters, One-stage op-amps, Two-stage op-amps, Gain Boosting, Common-mode feedback, Input range limitations, Slew Rate, Power supply rejection, Noise in op-amps	
	4.2	**Stability and Frequency Compensation:** General Considerations, Multipole systems, Phase margin, Frequency compensation, compensation of two stage op-amps	
5.0		**Mixed Signal Circuits**	10
	5.1	**Switch Capacitor Circuits:** MOSFETs as switches, Speed considerations, Precision Considerations, Charge injection cancellation, Unity gain buffer, Non-inverting amplifier and integrator	
	5.2	**Oscillators:** General considerations, Ring oscillators, LC oscillators, VCO	
	5.3	**Phase-Locked Loop:** Simple PLL, Charge pump PLL, Nonideal effects in PLL, Delay locked loops and applications of PLL in integrated circuits	
6.0		**Analog Layout and other concepts**	04
	6.1	**Analog Layout Techniques:** Antenna effect, Resistor matching, capacitor matching, current mirror matching, floorplanning, shielding and guard rings	
	6.2	AMS design flow, ASIC, Full custom design, Semi custom design, System on Chip, System in package, Hardware software co-design	
		Total	**52**

Recommended Books:

1. B Razavi, "*Design of Analog CMOS Integrated Circuits*", Tata McGraw Hill, 1st Edition.
2. R. Jacaob Baker, Harry W. Li, David E. Boyce, "*CMOS Circuit Design, Layout,and Stimulation*", Wiley, Student Edition
3. P. E. Allen and D. R. Holberg, "*CMOS Analog Circuit Design*", Oxford University Press, 3rd Edition.
4. Gray, Meyer, Lewis, Hurst, "*Analysis and design of Analog Integrated Circuits*", Willey, 5th Edition

Internal Assessment (IA):

Two tests must be conducted which should cover at least 80% of syllabus. The average marks of both the test will be considered as final IA marks

End Semester Examination:

1. Question paper will comprise of 6 questions, each of 20 marks.
2. Total 4 questions need to be solved.
3. Question No.1 will be compulsory and based on entire syllabus wherein sub questions of 2 to 5 marks will be asked.
4. Remaining questions will be selected from all the modules