204185 Digital Electronics

Teaching Scheme:

Lectures: 4 Hrs/ Week

Practical : 2 Hrs/week

Examination Scheme:

Theory Online : 50 Marks

Theory Paper : 50Marks

Practical: 50 Marks

Course Objectives and Outcomes:

The concept and theory of digital Electronics are needed in almost all electronics and telecommunication engineering fields and in many other engineering and scientific disciplines as well. The main objective of this course is to lay the foundation for further studies in areas such as communication, VLSI, computer, microprocessor etc. One of the most important reasons for the unprecedented growth of digital electronics is the advent of integrated circuit. This course will explore the basic concepts of digital electronics.

Having successfully completed this course, the student will be able to:

1. Understand the basic logic gates and various variable reduction techniques of digital logic circuit in detail.
2. Understand, identify and design combinational and sequential circuits
3. Design and implement hardware circuit to test performance and application for what it is being designed.
4. Simulate and verify using computer simulation software to obtain desired result.
5. Understand and verify simulated circuit model with hardware implementation.

Unit I: Digital Logic Families **8L**

Classification of logic families, Characteristics of digital ICs-Speed of operation, power dissipation, figure of merit, fan in, fan out, current and voltage parameters, noise immunity, operating temperatures and power supply requirements.TTL logic. Operation of TTL NAND gate, active pull up, wired AND, open collector output, unconnected inputs. Tri-State logic. CMOS logic – CMOS inverter, NAND, NOR gates, unconnected inputs, wired logic , open drain output. Interfacing CMOS and TTL. Comparison table of Characteristics of TTL, CMOS, ECL, RTL, I2L, DCTL.

Unit II : Combinational Logic Design **8L**

Standard representations for logic functions, k map representation of logic functions (SOP m POS forms), minimization of logical functions for min-terms and max-terms (upto 4 variables), don't care conditions, Design Examples: Arithmetic Circuits, BCD - to – 7 segment decoder, Code converters. Adders and their use as subtractions, look ahead carry, ALU, Digital Comparator, Parity generators/checkers, Multiplexers and their use in combinational logic designs, multiplexer trees, Demultiplexers and their use in combinational logic designs, Decoders, demultiplexer trees. Introduction to Quine McCluskey method.

Unit III : Sequential Logic Design **8L**

1 Bit Memory Cell, Clocked SR, JK, MS J-K flip flop, D and T flip-flops. Use of preset and clear terminals, Excitation Table for flip flops. Conversion of flip flops. Application of Flip flops: Registers, Shift registers, Counters (ring counters, twisted ring counters), Sequence Generators, ripple counters, up/down counters, synchronous counters, lock out, Clock Skew, Clock jitter. Effect on synchronous designs.

Unit IV : State Machines **8L**

Basic design steps- State diagram, State table, State reduction, State assignment, Mealy and Moore machines representation, Implementation, finite state machine implementation, Sequence detector.

Unit V : Programmable Logic Devices and Semiconductor Memories- **6L**

Programmable logic devices: Detail architecture, Study of PROM, PAL, PLA, Designing combinational circuits using PLDs. General Architecture of FPGA and CPLD

Semiconductor memories: memory organization and operation, expanding memory size, Classification and characteristics of memories, RAM, ROM, EPROM, EEPROM, NVRAM, SRAM,DRAM,

Unit VI : Introduction to HDLs **7L**

Library, Entity, Architecture, Modeling styles, Data objects, Concurrent and sequential statements, Design examples, using VHDL for basic combinational and sequential circuits, Attributes (required for

practical) (Test benches and FSM excluded).

Text Books :

1. R.P. Jain , "Modern digital electronics" , 3rd edition , 12th reprint TMH Publication, 2007.
2. Stephen Brown, "Fundamentals of digital logic design with VHDL" 1st edition, TMH Publication 2002

Reference Books :

1. A. Anand Kumar, "Fundamentals of digital circuits" 1st edition, PHI publication, 2001
2. Wakerly Pearon, "Digital Design: Principles and Practices", 3rd edition, 4th reprint, Pearon Education, 2004
3. J. Bhaskar, "VHDL Primer" 3rd Edition.PHI Publication.
4. Mark Bach, "Complete Digital Design", Tata MCGraw Hill, 2005.
5. Volnei Pedroni, " Digital: Electronics and Design with VHDL", Elsevier

List of Experiments

All the following Practicals are mandatory.

1 Verify four voltage and current parameters for TTL and CMOS (IC 74LSXX, 74HCXX), (Refer Data-Sheet).

2 Study of IC-74LS153 as a Multiplexer. (Refer Data-Sheet).

- Design and Implement 8:1 MUX using IC-74LS153 & Verify its Truth Table.
- Design & Implement the given 4 variable function using IC74LS153. Verify its Truth-Table.

3 Study of IC-74LS138 as a Demultiplexer/ Decoder (Refer Data-Sheet).

- Design and Implement full adder and subtractor function using IC-74LS138.
- Design & Implement 3-bit code converter using IC-74LS138.(Gray to Binary/Binary to Gray)

4 Study of IC-74LS83 as a BCD adder,(Refer Data-Sheet).

- Design and Implement 1 digit BCD adder using IC-74LS83
- Design and Implement 4-bit Binary subtractor using IC-74LS83.

5 Study of IC-74LS85 as a magnitude comparator,(Refer Data-Sheet)

- Design and Implement 4-bit Comparator.
- Design and Implement 8-bit Comparator

6 Study of Counter ICs (74LS90/74LS93). (Refer Data-Sheet)

- Design and Implement MOD-N and MOD-NN using IC-74LS90 and draw Timing Diagram.
- Design and Implement MOD-N and MOD-NN using IC-74LS93 and draw Timing Diagram.

7 Study of synchronous counter

- Design & Implement 4-bit Up/down Counter and MOD-N Up/down Counter using IC-74HC191/IC74HC193. Draw Timing Diagram

8 Study of Shift Register (74HC194/74LS95), (Refer data-Sheet)

- Design and Implement Pulse train generator using IC-74HC194/IC74LS95 (Use right shift/left shift).
- Design and Implement 4-bit Ring Counter/ Twisted ring Counter using shift registers IC 74HC194/IC74LS95.

9 Write, simulate and verify, VHDL Code for four bit logical and arithmetic operations for ALU.

- Behavioral modeling
- Dataflow modeling

10 D FF and JK FF (With Synchronous and asynchronous reset input)

(Use Behavioral modeling)

- Write, simulate and verify, VHDL Code for D flip flop using Synchronous /asynchronous reset input
- Write, simulate and verify, VHDL Code for JK flip flop using asynchronous set /reset Input

11 Four bit ripple counter**.** (Use data flow/Structural modeling)

- Write, simulate and verify, VHDL code for four bit ripple up counter
- Write, simulate and verify VHDL code for four bit ripple up/down Counter using mode control.