VLSI Design & Technology(404181)

Teaching Scheme:
Lectures: 3 Hrs/ Week

Examination Scheme:
In Semester Assessment:
Phase I : 30
End Semester Examination:
Phase II: 70

Course Objectives:

- To study HDL based design approach.
- To learn digital CMOS logic design.
- To nurture students with CMOS analog circuit designs.
- To realize importance of testability in logic circuit design.
- To overview SoC issues and understand PLD architectures with advanced features.

Course Outcomes:

After successfully completing the course, students will be able to

- Model digital circuit with HDL, simulate, synthesis and prototype in PLDs.
- Understand chip level issues and need of testability.
- Design analog & digital CMOS circuits for specified applications.

Unit I : VHDL Modeling 7L

Data objects, Data types, Entity, Architecture & types of modeling, Sequential statements, Concurrent statements, Packages, Sub programs, Attributes, VHDL Test bench, Test benches using text files. VHDL modeling of Combinational, Sequential logics & FSM, Meta-stability.

Unit II : PLD Architectures 7L

PROM, PLA, PAL: Architectures and applications. Software Design Flow. CPLD Architecture, Features, Specifications, Applications. FPGA Architecture, Features, Specifications, Applications.

Unit III: SoC & Interconnect 6L

Clock skew, Clock distribution techniques, clock jitter. Supply and ground bounce, power distribution techniques. Power optimization. Interconnect routing techniques, wire parasitic, Signal integrity issues. I/O architecture, pad design. Architectures for low power.

Unit IV: Digital CMOS Circuits 7L

MOS Capacitor, MOS Transistor theory, C-V characteristics, Non ideal I-V effects, Technology Scaling. CMOS inverter, DC transfer characteristics, Power components, Power delay product.

Transmission gate. CMOS combo logic design. Delays: RC delay model, Effective resistance, Gate and diffusion capacitance, Equivalent RC circuits; Linear delay model, Logical effort, Parasitic delay, Delay in a logic gate, Path logical efforts.

Unit V: Analog CMOS Design 7L

Current sink and source, Current mirror. Active load, Current source and Push-pull inverters. Common source, Common drain, Common gate amplifiers. Cascode amplifier, Differential amplifier, Operational amplifier.

Unit VI : Testability 6L

Types of fault, Need of Design for Testability (DFT), Testability, Fault models, Path sensitizing, Sequential circuit test, BIST, Test pattern generation, JTAG & Boundary scan, TAP Controller.

Text Books

1. Charles H. Roth, “Digital systems design using VHDL”, PWS.
2. Wyane Wolf, “Modern VLSI Design (System on Chip)”, PHI Publication.

Reference Books

1. Allen Holberg, “Analog CMOS Design”, Oxford University Press.
2. Neil H. E. Weste, David Money Harris, “CMOS VLSI Design: A Circuit & System Perspective”, Pearson Publication