Lab Practice - II (404187)

VLSI and Elective I

Teaching Scheme: **Examination Scheme:** PR: 50Marks
Practicals: 4 Hrs/week TW:50Marks

VLSI

Experiments:

A. To write VHDL code, simulate with test bench, synthesis, implement on PLD. [Any 4].

1. 4 bit ALU for add, subtract, AND, NAND, XOR, XNOR, OR, & ALU pass.
2. Universal shift register with mode selection input for SISO, SIPO, PISO, & PIPO modes.
3. FIFO memory.
4. LCD interface.
5. Keypad interface.

B. To prepare CMOS layout in selected technology, simulate with and without capacitive load, comment on rise, and fall times.

1. Inverter, NAND, NOR gates, Half Adder
2. 2:1 Multiplexer using logic gates and transmission gates.
3. Single bit SRAM cell.
4. D flip-flop.

Elective I

Experiments to be chosen based on Elective I.