VLSI Design (404201)

Teaching Scheme:
Lectures: 3 Hrs/ Week

Examination Scheme:
In Semester Assessment:
Phase I : 30
End Semester Examination:
Phase II: 70

Prerequisite:

- Study of basic PLDs.
- Knowledge of VHDL.

Course Objectives:

- To understand CMOS and its application in VLSI Circuits.
- To design digital circuits using VHDL.
- To implement digital circuits using CPLD/FPGA.
- To detect faults in the design.

Course Outcomes:

After successfully completing the course students will be able to

- Understand VLSI Design Flow.
- Design any digital circuit using VHDL.
- Understand the importance of testability in chip design.

Unit I : Introduction to VLSI Circuits 7L

Introduction to MOSFETs**:** MOS Transistor Theory –Device Structure and Physical Operation, Current Voltage Characteristics, Fabrication, MOS Capacitor, Body Effect, Temperature Effects, Channel Length Modulation, Latch-up.
MOS Inverter: MOS Transistors, MOS Transistor Switches, CMOS Logic, Circuit and System Representations, Design Equations, Transistor Sizing, Voltage Transfer Characteristics, Power Dissipation, Noise Margin, Power Delay Product, Energy dissipation.
MOS Layers Stick/Layout Diagrams; Layout Design Rules, Issues of Scaling, Scaling factor for device parameters. Combinational MOS Logic Circuits: Pass Transistors/Transmission Gates; Designing with transmission gates: Primitive Logic Gates.

Unit II : Digital Circuit Design using VHDL 7L

Design of sequential circuits, asynchronous and synchronous design issues, state machine modeling (Moore and mealy machines), packages, sub programs, attributes, test benches.

Unit III : Programmable Logic Devices 6L

Complex Programmable Logic Devices – Architecture of CPLD, Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable

Interconnects, Programmable I/O blocks in FPGAs, Dedicated Specialized Components of FPGAs, and Applications of FPGAs.

Unit IV : CMOS Subsystem Design 6L

Semiconductor memories, memory chip organization, Random Access Memories (RAM), Static RAM (SRAM), standard architecture, 6T cell, sense amplifier, address decoders, timings. Dynamic RAM (DRAM), different DRAM cells, refresh circuits, timings.

Unit V : Floor Planning and Placement 6L

Floor planning concepts, shape functions and floor plan sizing, Types of local routing problems Area routing, channel routing, global routing, algorithms for global routing.

Unit VI : Fault Tolerance and Testability 6L

Types of fault, stuck open, short, stuck at 1, 0 faults, Fault coverage, Need of Design for Testability (DFT), Controllability, predictability, testability, built in Self Test (BIST), Partial and full scan check, Need of boundary scan check, JTAG, Test Access Port (TAP) controller.

Text Books

1. Neil H. Weste and Kamran, Principles of CMOS VLSI Design, Pearson Publication
2. John F. Wakerly, Digital Design, Principles and Practices, Prentice Hall Publication

Reference Books

1. Douglas Perry, VHDL, McGraw Hill Publication.
2. Charles Roth, Digital System Design using VHDL, McGraw Hill Publication.
3. Data Sheets of PLDs.
4. Sung-Mo (Steve) Kang, Yusuf Leblebici, CMOS Digital Integrated Circuits, Tata McGraw Hill Publication.