DSP Processors (404205)

Teaching Scheme:
Lectures: 3 Hrs/ Week

Examination Scheme:
In Semester Assessment:
Phase I : 30
End Semester Examination:
Phase II: 70

Course Outcomes:
The student will be able to

1. Write different digital processing algorithms.
2. Show skills to design of filters for real time application.
3. Exhibit the knowledge of DSP algorithms on DSP Platforms.
4. Demonstrate the ability to analyze filter structures

Unit I : **Introduction to real time digital signal processing** 6L

Basic elements of real time DSP, The sampling process, Discrete time sequences. Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear time-invariant systems, Digital filters, Decimation and interpolation, Analysis and Design tool for DSP Systems, computational accuracy in DSP implementations: Number formats for signals and coefficients in DSP systems, Dynamic Range and Precision, Sources of error in DSP implementations, A/D Conversion errors, DSP Computational errors, D/A Conversion Errors, Compensating filter.

Unit II: **Architectures for programmable DSP devices** 6L

Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation Unit, Programmability and Program Execution, Speed Issues, Features for External interfacing. Execution control and pipelining: Hardware looping, Interrupts, Stacks, Relative Branch support, Pipelining and Performance, Pipeline Depth, Interlocking, Branching effects, Interrupt effects, Pipeline Programming models.

Unit III**: Programmable digital signal processors** 6L

Selections of DSP processors, real time implementation considerations, Hardware interfacing, addressing modes and DSP processor architectures: TMS 320C54XX, TMS 320C67XX, Blackfin processor: Architecture overview, memory management, I/O management, On chip resources, programming considerations, Real time implementations, Code Optimization

Unit IV : **Implementations of DSP Algorithms** 6L

The Q-notation, FIR Filters, IIR Filters, Interpolation Filters, Decimation Filters, PID Controller, Adaptive Filters, 2-D Signal Processing.

Unit V: **Implementation of FFT algorithms** 6L

An FFT Algorithm for DFT Computation, A Butterfly Computation, Overflow and scaling, Bit-Reversed index generation, An 8-Point FFT implementation on the TMS320C54XX, Computation of the signal spectrum.

Unit VI: **Interfacing with programmable DSP devices** 6L

Memory space organization, External bus interfacing signals, Memory interface, Parallel I/O interface, Programmed I/O, Interrupts and I/O, Direct memory access (DMA). A Multichannel buffered serial port (McBSP), McBSP Programming, CODEC interface circuit, CODEC programming, A CODEC-DSP interface.

Text Books

1. Avtar Singh and S. Srinivasan "Digital Signal Processing ", Thomson Publications, 2004.
2. Sen M. Kuo and Woon-Seng Gan, " Digital Signal Procesors, architectures, implementations, and applications", Prentice-Hall, ISBN 0130352144.

Reference Books

1. Lapsley et al. "DSP Processor Fundamentals, Architectures & Features", S. Chand & Co, 2000.
2. B. Venkata Ramani and M. Bhaskar, "Digital Signal Processors, Architecture, Programming and Applications –", TMH, 2004.
3. Jonathan Stein "Digital Signal Processing", John Wiley, 2005